REMARKS

Prior to the present amendment, claims 1-7, 9, 11, 13, and 20-23 were pending in the present application and remain pending in the present application. By the present amendments, Applicant has added new claims 30-35. Thus, after the present amendments and response, claims 1-7, 9, 11, 13, 20-23, and 30-35 are pending in the present application. Reconsideration of claims 1-7, 9, 11, 13, and 20-23 and allowance of all pending claims 1-7, 9, 11, 13, 20-23 and 30-35 in view of the above amendments and the following remarks are requested.

A. Rejection of Claims 1-7, 9, 11, 13, and 20-23 under 35 USC §103(a)

The Examiner has rejected claims 1-7, 9, 11, 13, and 20-23 under 35 USC §103(a) as being unpatentable over United States Patent Number 6,740,952 B2 to Fujishima et al. (hereinafter "Fujishima") in view of United States Patent Number 6,525,390 B2 to Tada et al. (hereinafter "Tada"); United States Patent Number 6,639,277 B2 to Rumennik et al. (hereinafter "Rumennik"); *Microchip Fabrication: A Practical Guide to Semiconductor Processing*, 2000, Mc-Graw Hill, New York, 4th Edition, pp. 382,511, by Peter Van Zant (hereinafter "Van Zant"); *VLSI Fabrication Principles: Silicon and Gallium Arsenide*, 1994, John Wiley & Sons, Inc., New York, 2nd Edition, pp. 258-259, by Sorab K. Ghandhi (hereinafter "Ghandhi"); United States Patent Number patent number 6,617,652 B2 to Masaaki Noda (hereinafter "Noda"); and United States Patent Number patent number 5,801,431 to Niraj Ranjan (hereinafter "Ranjan"). For the reasons discussed

below, Applicant respectfully submits that the present invention, as defined by independent claim 1, is patentably distinguishable over Fujishima, Tada, Rumennik, Zant, Ghandhi, Noda, and Ranjan, either singly or in any combination thereof.

Independent claim 1 recites a semiconductor device with a novel field plate structure. The field plate structure is disposed over a reduced surface field ("resurf") region on the device and includes a first a first field plate disposed over a first insulation layer of a first thickness extending from said gate insulation layer. *See* claim 1 above. The field plate structure further includes a second field plate disposed over a second insulation layer of a second thickness, where the second insulation layer is formed over the first insulation layer. *See id.* The field plate structure also includes a third field plate spaced from the second field plate by a third insulation layer of a third thickness, where the first field plate includes a first portion spaced from a second portion by a first gap, and the first portion of the first field plate extends from the gate electrode. *See id.*

In claim 1, the second portion of the first field plate is electrically connected to the drain region and the second field plate includes a first portion spaced from a second portion by a second gap. *See id.* The third field plate includes a first portion spaced from a second portion by a third gap, and the first gap is wider than the second gap and the third gap, and the second gap is wider than the third gap. *See id.* The gaps are filled only with an insulation material and the first portion and the second portion of the second field plate, and the first portion and the second portion of the third field plate are disposed

around the drain region. *See id.* As noted in claim 1, the semiconductor device exhibits a breakdown voltage of at least 600 volts. *See id.*

As disclosed in the present application, published as publication number U.S. 2004/0201078 A1 (hereinafter the "Application), in an embodiment of the invention, a field plate structure is formed over resurf region 30, where the field plate structure includes a first field plate having first portion 32 and second portion 33 spaced from its first portion 32 by gap 39, a second field plate having first portion 36 and second portion 38 spaced from its first portion 36 by gap 40, and a third field plate having first portion 42 and second portion 44 which is spaced for first portion 42 by gap 46. See, e.g., Figure 1 and related text of the Application.

As further disclosed in the Application, the first field plate structure is disposed over resurf region 30, which is formed in epitaxially formed semiconductor layer 12 between drain region 26 and body region 14 over at least a portion of drift region 28, where second portion 33 of the first field plate is electrically connected to drain region 26 by electrical connectors 50 and second portion 38 of the second field plate structure. *See*, e.g., Figure 1 and related text of the Application. As disclosed in the present application, a field plate according to the present invention reduces the surface charge on the field insulation beneath each plate to advantageously permit the devices to withstand 650 V or more when applied in, for example, 0.35 micron CMOS. *See*, e.g., paragraph [0012] of the Application.

Applicant respectfully submits that the present invention is nonobvious over the cited art for at least several reasons. First, Applicant submits that the Examiner has not shown *prima facie* obviousness because the Examiner has not taken the invention as a whole as required by the Manual of Patent Examining Procedure (hereinafter "MPEP"). *See*, e.g., MPEP § 2142. Rather, Applicant submits that the Examiner has conflated the obviousness inquiry by separating distinct features of claim 1 and finding each individual feature obvious in view of a patchwork of references.

For example, the Examiner has conceded that the resurf region of the present invention is not taught by Fujishima, but is obvious in view of Tada. *See* Office Action dated October 15, 2009 at 5. The Examiner has similarly conceded that the plate spacing of the present invention is not taught by Fujishima, but is obvious in view of Rumennik. *See id.* at 5-6. Moreover, the Examiner has conceded that the epitaxial layer of the present invention is not taught by Fujishima, but is obvious in view of Rumennik, Ghandhi and Van Zant. *See id.* at 6. Finally, the Examiner has conceded that the connection of the second and third plates to the drain region is not taught by Fujishima, but is obvious in view of Noda and Ranjan. *See id.* at 6-7.

Applicant submits that the Examiner has evaluated only individual features of the present invention and has not construed the present invention as a whole. To this end, Applicant submits that the Examiner has argued that Fujishima teaches "most aspects of the invention." The Examiner's citation to "aspects" of the invention and not the invention as a whole indicates that the Examiner has pieced together distinct attributes of

the present invention to find obviousness instead of predicating obviousness on the structures and functions of the invention as a whole. As such, Applicant submits that the Examiner has not shown *prima facie* obviousness and that the present invention is therefore nonobvious over the cited art.

Second, Applicant submits that the resurf region of the present invention makes the present invention nonobvious over the cited art. Applicant notes that the Examiner has conceded that Fujishima does not teach a resurf region. *See* Office Action dated October 15, 2009 at 5. Applicant further submits that counter-doped region 44 of Tada cannot be interpreted as a resurf region. As defined in the art, a resurf region is a lightly doped and relatively shallow region that is substantially depleted of free charge carriers before the adjoining pn junction is reverse biased thereby spreading the surface electric field and increasing the reverse breakdown voltage of the pn junction. In Tada, counter-doped region 44 is formed by counter-doping p-type impurities to the surface portion of n-type offset region 3 formed in substrate 1. *See*, e.g., Figures 9 and 10 and related text of Tada. Counter-doped region 44 has a p-type impurity concentration of $3x10^{16}$ cm^{-3}. *See*, e.g., column 12, lines 17-28 of Tada. Applicant respectfully submits that counter-doped region 44 of Tada is not lightly doped nor is it sufficiently shallow to constitute a resurf region. Accordingly, Applicant submits that the resurf region of the present invention makes the present invention nonobvious over the cited art.

Third, Applicant respectfully submits that the spacing of the first and second field plates and the connection of the second portion of the first plate to the device drain make

the present invention nonobvious over Fujishima in view of Rumennik. As noted above, the first field plate of claim 1 includes a second portion that is spaced from a first portion by a first gap that is wider than the gap spacing the first and second portions of the second field plate. Applicant submits that Rumennik does not teach this feature. More specifically, Applicant submits that the spacing of source 10 and drain 11 in Rumennik cannot be interpreted as the spacing of a field plate. As recited in claim 1, a field plate is distinct from the separately recited source and drain regions. *See* claim 1 above. Figure 1 of the Application illustrates source region 18 and drain region 26 as regions that are distinct from field plates 23, 33, 36, 38, 42 and 44. *See* Figure 1 of the Application. Applicant therefore submits that one of ordinary skill in the art would not have interpreted the drain source gap in Rumennik to teach a field plate gap as recited in the present invention.

Finally, Applicant submits that the Examiner's reasoning is based on an impermissible hindsight reconstruction of the present invention. Although the tendency to resort to hindsight based upon an applicant's disclosure is often difficult to avoid due to the very nature of the examination process, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art. *See* MPEP § 2142. Applicant respectfully submits that a person of ordinary skill in the art, at the time the invention defined by amended independent claim 1 was made, would have not reasonably combined Fujishima, Tada, Rumennik, Zant, Ghandhi, Noda, and Ranjan, as suggested by the Examiner. Thus, Applicant submits that the teachings

suggested by the Examiner (i.e. the combination of Fujishima, Tada, Rumennik, Zant, Ghandhi, Noda, and Ranjan) are based on an impermissible hindsight reconstruction given the benefit of Applicant's disclosure.

For all the foregoing reasons, Applicant respectfully submits that, at the time the invention defined by amended independent claim 1 was made, the invention would not have been obvious to a person of ordinary skill in the art by Fujishima, Tada, Rumennik, Van Zant, Ghandhi, Noda, and Ranjan, either singly or in any combination thereof. Thus, amended independent claim 1 is patentably distinguishable over Fujishima, Tada, Rumennik, Van Zant, Ghandhi, Noda, and Ranjan and, as such, claims 2-7, 9, 11, 13, and 20-23 depending from amended independent claim 1 are, *a fortiori*, also patentably distinguishable over Fujishima, Tada, Rumennik, Van Zant, Ghandhi, Noda, and Ranjan for at least the reasons presented above and also for additional limitations contained in each dependent claim. Accordingly, Applicants respectfully request allowance of claims 1-7, 9, 11, 13 and 20-23.

B. <u>New Claims 30-35</u>

By the present amendment, Applicant has added new claims 30-35. Applicant respectfully submits that new claims 30-35 are patentably distinguishable over the cited art. Applicants therefore request allowance of claims 30-35.

C. Conclusion

For all the foregoing reasons pending 1-7, 9, 11, 13, and 20-23 are patentably distinguishable over the cited art, and an early allowance of all claims 1-7, 9, 11, 13, 20-23, and 30-35 is respectfully requested.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.